1 Thesis Project: Low-latency techniques as applied to price adjustments following a large trade

1 student

**Background:** For any instrument or market, a large block trade will typically be followed by an adjustment process as the market responds to the trade. Prior work (Cummings, Frino 2009) suggests that large trades stimulate subsequent activity as traders interpret the price implication of the trade.

**Part 1:** Characterize adjustment process following a large block trade.

Greater liquidity generally results in a faster normalization response following a large block trade. Identify a foreign exchange instrument to target for this study. Trace the bid-ask spreads following a large trade. Separate traces by order size, contract expiration date, purchases vs sales. Compare results using different time scales (for lower granularity, successive trades are lumped together). How does the spread renormalize? Cummings/Frino present averaged results from 10 years of data. Trace some individual trades.

**Part 2:** How can low-latency arbitrage techniques be applied to the adjustment process?

Examine market response of related instruments. Identify any correlations in market activity. How does the renormalized spread compare to related instruments? Because volatility increases after a large block trade, identify opportunities to capture price swings.

**Expansion:** The results of this project can be applied to creating predictive models of customer order flow for foreign exchange price forecasting. Alternately, the results can be implemented as algorithmic trading techniques realized in hardware in order to verify the effectiveness of the strategies identified in Part 2.

2 Thesis Project: Ultra-low latency execution for deterministic arbitrage trading strategies on ASX

1 student

**Background:** Deterministic arbitrage involves buying an underpriced asset in one market and short-selling an overpriced related asset or instrument in another market. Assuming the prices will eventually converge to a correct and equal value, a profit will be earned with minimal risk. In an efficient market, these opportunities are very rare. However, it is possible to indirectly determine an asset’s value by finding a related instrument. Statistical arbitrage opportunities can arise when price discrepancies are estimated using some underlying model for the expected value. Using ultra-low latency strategies, it may be possible to exploit existing deterministic arbitrage opportunities or execute statistical arbitrage strategies with minimal risk.

Build an ASX market model incorporating parallel trading agents based on our existing knowledge of the various latency components of the ASX platform (the framework has already been laid out in Modula-3).

For selected instruments or securities, obtain historical tick data from [https://ausequities.sirca.org.au/](https://ausequities.sirca.org.au/). Run the data through the simulated trading agents while monitoring arbitrage opportunities. Determine the minimum trade execution latency required to exploit deterministic arbitrage opportunities, if any. Develop statistical arbitrage strategies with very simple valuation models, assuming ultra-low latency execution.

**Expansion:** Repeat this study using KRX or HKE market models, if latency parameters and market data are available. Compare minimum latency requirements for successful execution of arbitrage strategies with market liquidity.
Implement some statistical arbitrage strategies on the NetFPGA platform. Run test cases to measure actual roundtrip time from receipt of market data to order placement. Optimise trading strategies for sufficiently low latency and minimal risk based on historical data.

If there is sufficient time remaining, TCP/IP hardware optimisation techniques could even be explored and implemented in the NetFPGA platform to really measure the lowest achievable latency.

3 Thesis Project: Characterization of 3D Hybrid FPGAs with resistance-change memory cells

1-2 students

Background: Resistance-change memory cells are two-terminal non-volatile devices that can be programmed to maintain a high-resistance state or a low-resistance state. Hybrid FPGA architectures can be built that use these resistance-change memory cells as switches with interconnect. A hybrid FPGA architecture maintains arrays of logic gates in the CMOS substrate, but routing and configuration are controlled in the interconnect using multiple layers of dense wires. Resistance-change materials can be deposited above the silicon substrate at the cross-points of metal wires, serving as two-terminal switching devices. Because metal wires and switching devices can be monolithically stacked, it is possible to build a 3-dimensional interconnect hierarchy to configure logic designs in the architecture.

Create a logic tile consisting of one logic block, two intersecting interconnect channels (connection blocks), and one switchblock. Design an equivalent logic tile using resistance-change switches. Entire FPGAs can be generated for each design by repeating the layout of a single tile.

Extract wire lengths, parasitic resistance and capacitance values from tile layouts. Estimate the delay time between logic blocks through simulation. Sweep multiple layers of switches in a switchblock tile. Compare performance to standard FPGA logic tile.

Expansion: Examine other factors such as signal degradation due to nonideal switches, parasitic capacitance, 3-dimensional design architectures.