Characterizing Drain Current Dispersion in GaN HEMTs with a New Trap Model

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Abstract— Dispersio in a GaN HEMT, including gate and drain lag, is related to a new trapping model based on SRH theory. The model is used to explain the bias- and terminal-potential dependency of the turn-on transients and their time constants. Because the time constants are extremely long they impact the measurement of true dc characteristics and contribute to knee walk-out. Temperature as a function of time is shown to be a vital consideration. The models of both drain current and trapping need to consider temperature and power dissipation versus time. The relationship between trap potentials and terminal potentials is investigated.

I. INTRODUCTION

Charge trapping, and its manifestation of current lag, is present in compound-semiconductor HEMTs. The problem is that dc characteristics are not representative of high-frequency operation because of anomalous effects of which some are referred to in the literature as dispersion [1], current slump [2], current compression [3], power slump [4], knee walk-out [5], and gate lag [6]. Charge trapping, which occurs in both GaAs and GaN technologies, is responsible for most of these. The observed current collapse is attributed to surface and substrate trapping and this can be more pronounced in GaN devices [7]. For GaN, obtaining true dc characteristics is problematic because the time constants can be many thousands of seconds. It is necessary, for design and application of these devices, to quantify the relationship between high-frequency characteristics and the near-dc characteristics that are measured in practice.

Recently, a new model of a trap centre based on Shockley-Read-Hall (SRH) theory was proposed [8]. This model can be used to predict dispersion of large-signal characteristics versus frequency and bias. The model can be parameterised with pulse and time-evolution measurements [9].

In this paper, time-evolution measurements and insight from the SRH trap model are used to analyse trapping effects. Section II examines the effects of trapping in a GaN HEMT shown in a series of time-evolution measurements. Section III summarises the new trap model while Section IV uses this model to discuss the experimental results, and finally Section V draws some conclusions.

II. DRAIN CURRENT DISPERSION

Dispersion in the drain-source current characteristic of a Nitronex NTB00025 GaN HEMT is shown in Figs 1 and 2. Figure 1 shows the dramatic dependence of the drain current characteristic on the rate of its measurement and on the quiescent condition established prior to the measurement. A quiescent bias well beyond pinch-off causes a significant reduction in drain current that is still observed one second after turn-on. Recovery from this slump is observed for most drain potentials after 1000 seconds. A longer time is required at low potentials. The dependence of this recovery time on drain potential can be observed in a time-evolution measurement.

A. Time-evolution Measurement

A time-evolution measurement of the GaN HEMT is shown in Fig. 2, which shows a surface of drain current versus log-time and drain potential for a constant gate potential. Each point was measured after holding a quiescent condition for 1000 s at $V_{GSQ} = -2$ V and $V_{DSQ} = 0$ V and at $V_{GSQ} = -6.0$ V and $V_{DSQ} = 0$ V.

Fig. 1. Drain current characteristic of a Nitronex NTB00025 GaN HEMT with pinch-off at $V_{GS} = -1.9$ V. The measurement is recorded after 1 s or 1000 s at $V_{GS} = -1.5$ V and drain potentials from 0 V to 17 V. Each point was measured after holding a quiescent condition for 1000 s at $V_{GSQ} = -2.0$ V and $V_{DSQ} = 0$ V and at $V_{GSQ} = -6.0$ V and $V_{DSQ} = 0$ V.
a specific quiescent condition. Each line in Fig. 2 is a transient response for a step change from the quiescent condition to the establishment of a new dc condition. It is characterised by:

- An initial drain current immediately after the step change, \( I_{DSI} \)
- A final drain current at the end of the transient, \( I_{DSF} \)
- The time-constant associated with the transient response

The time-evolution surface in Fig. 2 is one of many that were gathered for this device from a range of quiescent conditions. The surface shown is typical of these and some data from the other measurements are shown in the later Figures. From this study, it is confirmed that the time-constants and initial currents vary significantly with the quiescent point, \( V_{GSQ} \) and \( V_{DSQ} \), and with the time that this quiescent point was maintained. That is, the characteristics of the time-evolution surface are history dependent.

Although there is also some variation in the surface with the gate potential that is stepped to, the following will focus on a current-lag scenario. The notable feature of interest is a delayed increase in current.

**B. Current Lag**

When the gate-source potential is stepped without changing the drain-source bias, there is a component of drain-source current, \( I_{DS} \), that lags the causal change in the gate-source potential. This is often referred to as gate lag. Similarly, when the drain-source potential is stepped without changing the gate-source potential there is a component in \( I_{DS} \) that lags, which is referred to here as drain lag. Figure 2 shows the case when both gate-source and drain-source potentials are changed, which gives a combination of gate and drain lag.

Fig. 3 shows the change in drain current, \( I_{DS} \), with time after a turn-on to \( V_{GS} = -1.5 \) V from various quiescent gate potentials, \( V_{GSQ} \), from \(-2\) V and \(-12\) V. The device was held at quiescent for 1000 seconds before each step response was measured. The drain-source potential was unchanged at 9 V.

The response in Fig. 3 is that of gate-lag. Three behavioural features are evident here. Firstly, the more heavily the device is pinched off at quiescent, the more reduced is the initial drain current, \( I_{DSI} \), immediately after turn on and secondly, the longer is the delay before the final rise to \( I_{DSF} \). Thirdly, the transient is nearly that of a first-order response but varies with the depth of pinch-off at quiescent. It is a sub-first-order for shallow pinch-off where the initial current is higher and it is greater than first-order after deep pinch-off where the initial current is lower.

Other measurements were made to examine the dependency of the change in \( I_{DS} \) with time on the quiescent drain-source potential. Figure 4 illustrates a comparison between two lines in Fig. 3, which are from \( V_{DSQ} = 9 \) V, and the case for \( V_{DSQ} = 17 \) V. The response in the latter case will be a combination of both gate-lag and drain-lag. The results
show that a higher $V_{DSQ}$ lowers the initial drain current $I_{DSI}$ and lengthens the delay before the rise to $I_{DSF}$.

III. SRH Trap Model

Trap centres within field-effect transistors affect their channel properties such that the drain-source current $I_{DS}$ is a function of its terminal potentials ($V_{GS}$ and $V_{DS}$) and the potentials at the trap site. The latter are a function of the polarity and charge state of the traps. A donor trap is neutral when occupied by electrons and positively charged when empty. An acceptor trap is neutral when it is empty and negatively charged when occupied by electrons. There can be donor or acceptor traps in the surface or substrate regions and the position affects their dependence of their charge state on the terminal potentials.

To account for the influence of a trap centre, it has been proposed that the drain current be considered a function of the trap potential, $v_T$, that adds to the gate potential as in [8]:

$$I_{DS} = f(V_{GS} + v_T, V_{DS}).$$

(1)

Since the gate and drain potentials are constant after a step or turn-on transient, the change in $I_{DS}$ from $I_{DSI}$ to $I_{DSF}$ is a result of a change in the trap potential term in (1). This trap potential and its rate of change needs to be considered as a function of $V_{GSQ}, V_{GS}, V_{DSQ}, V_{DS}$ and of time.

It has been demonstrated that a trap centre can be modelled by a capacitor that is charged by two types of current sources: an emission current, $i_E$, that represents the process of charge emission; and a capture current, $i_C$, that represents the process of charge capture [8]. Both currents are functions of the trap potential and the capture current is a function of the operating condition of the FET. This representation is shown in the circuit model of in Fig. 5. In this Figure, $i_T$ represents the trap current responsible for charging the capacitor, $C_T$. The term $v_T$ is the trap-control potential that controls the capture process. The trap potential, $v_T$, is simply the potential across the capacitor. Under steady-state conditions, the trap potential, $v_T$, is given by (25) in [8] as:

$$v_T = \frac{V_T}{1 + \exp \left( \frac{V_T}{kT} \right)},$$

(2)

where $V_T$ [V] is the trap potential when it is fully ionized, $T$ [K] is temperature, and $k$ [eV/K] is the Boltzman constant. The dependence of the trap potential in (1) on the terminal potentials is implemented by setting the trap-control potential to be a function of the terminal potentials.

According to the measured data, the trap-control potential of a FET, which is a two terminal potentials device, needs to be a nonlinear function of its terminal potentials. A simple alternative is modification to the trap model in [8] proposed here and shown in Fig. 5. This is the addition of a capture current for each potential as:

$$i_C = (i_{C,GS} + i_{C,DS}).$$

(3)

Setting each capture current to a nonlinear function of one terminal potential leads to the following relationship for trap potential under steady-state conditions:

$$v_T = \frac{V_T}{1 + \exp \left( \frac{\alpha_1 V_{GS} + \beta_1}{kT} \right) + \exp \left( \frac{\alpha_2 V_{DS} + \beta_2}{kT} \right)},$$

(4)

where $\alpha_1, \alpha_2, \beta_1$ and $\beta_2$ are fitting parameters.

In this modified representation, gate-lag and drain-lag are associated with each capture source independently. This simplifies the parameterisation of the model from transient response measurements.

It is clear from (4) that the quiescent trap potential is set by the quiescent terminal potentials. This will be the trap potential immediately after a step change, and this will set the initial drain current in (1). After sufficient time to charge the trap the steady-state trap potential will be established, which will be that set by the terminal potentials stepped to. This, in conjunction with any temperature changes related to power dissipation, sets the final drain current.

A. Time Constant

The dependence of the trap potential on time is predicted by the time-constant of the trap model. The capture and emission rates are determined by the dynamic resistances of the sources, which are all functions of the trap potential and temperature. The trap response rate will vary depending on which of capture or emission is dominant [8].

The capture rate after a step change is a function of the trap-control potentials that are stepped to. It is independent of their value before the step. This might imply that the time constant associated with the transient response of drain-current dispersion is independent of quiescent condition. However, there is a significant variation of trapping rates with temperature, which are dependent on changing power dissipation. The rates are proportional to $T^2 \exp(-E_A/kT)$ where $E_A$ is the activation energy for the trap [8].

IV. DISCUSSION

The dependency of drain-current turn-on response on the quiescent condition is shown in Figs 3 and 4 for various quiescent points and a fixed destination bias point. There is clear evidence of a variation in current recovery rates with quiescent condition. The trap model, which is based on SRH theory, shows that this is not related to the potentials of the quiescent
point. This implies that the changing rates are related to the variations in how temperature changes. Temperature is related to power dissipation [10]. The power dissipations associated with the initial drain currents, \( I_{DSI} \), are significantly different for each quiescent case in Fig. 3.

For \( V_{GSQ} = -12 \) V, the initial drain current is significantly lower, so the initial power dissipation is also significantly lower. Thus the initial temperature rise prior to the drain-current rise is lower compared to the other cases. This gives a slower trapping rate but once the current does rise, the temperature and hence trap speed transition improve or less at the last moment. The result is a response that is greater than first-order because both trapping and heating are interacting simultaneously. The response for \( V_{GSQ} = -2 \) V is sub-first order because there is less change in power dissipation as the drain-current rise progresses, so the sub-first-order heating response is progressively affecting trapping rates. These observations demonstrate that temperature is a vital consideration in transient response.

The fitting parameters in (4) can be determined from the change in initial and final drain currents. The difference between these can be related to the corresponding change in trap potential as:

\[
\Delta V_T = \frac{I_{DSF} - I_{DSI}}{g_m}, \quad (5)
\]

where \( g_m \) is the transconductance of the transistor. Figure 6 shows measurements of the current difference for a fixed destination bias point of \( V_{DS} = 9 \) V and \( V_{GS} = -1.5 \) V, measured from a range of quiescent points (held for 1000 s) of \( V_{GSQ} \) between \(-12 \) V and \(-2 \) V, and \( V_{DSQ} \) between 9 V and 17 V. This shows a nonlinear relationship between quiescent terminal potentials that can be predicted by (4).

A plausible explanation for the observed trap potential is that a normally ionized donor trap is neutralized by electron injection when there is a negative gate-potential quiescent condition. This injection increases at deeper pinch-off but is decreased by lateral fields generated by high drain potentials. This case is predicted by (4) with \( V_T < 0, \alpha_1 < 0, \) and \( \alpha_2 > 0 \). The corresponding trap potential predicted by (4) is shown in Fig. 6. The measured results fit a region of this surface very well. There is a variation with time spent at quiescent that can quantify and separate capture and emission processes from which the trap polarity can be confirmed.

V. CONCLUSION

It has been demonstrated that dispersion in a GaN HEMT can be related to trapping effects. These have extremely long time constants, which impacts the measurement of true dc characteristics. A trap model has been used to explain the bias-and-terminal-potential dependency of turn-on transients. From the model, it was concluded that temperature is a vital consideration. Both the transistor’s drain current and trap model need to consider temperature as a function of time. The relationship between trap potentials and terminal potentials has been investigated. This is a key consideration for the prediction of the extent and nature of dispersion relative to bias and operating conditions.

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REFERENCES


![Fig. 6. Trap potential versus terminal potential. The surface is calculated from (4) with \( \alpha_1/(kT) = 0.35, \beta_1/(kT) = -1 \) V, \( \alpha_2/(kT) = 0.4 \), and \( \beta_2/(kT) = -7 \) V. The measured points are derived from time-evolution data and fit a region of the theoretical surface very well. There is an offset related to transconductance and \( V_T \) included in this data.](image-url)